

Claims

What I claim is:

[0024] 1. An integrated circuit formed on a semiconductor wafer having a

first surface separated from a second surface and edges, comprising:

5 a region separating said integrated circuit from neighboring integrated
circuits;

one or more contact pads within said integrated circuit on said first
surface;

one or more electrically conductive materials placed in communication

10 with said bonding pad; and

said electrically conductive materials making contact to said second
surface or said region.

[0025] 2. The integrated circuit of claim 1 wherein a barrier material is placed between
said conductive materials and said integrated circuit body.

15 [0026] 3. The integrated circuit of claim 1 wherein said conductive material surrounded
by said barrier material is contained in a channel in said semiconductor
wafer and said channel connects said front surface bonding pad to
said second surface or said separation region.

[0027] 4. An integrated circuit formed on a semiconductor wafer having a

20 first surface separated from a second surface by a known thickness
and edges, comprising:

a region separating said integrated circuit from neighboring integrated
circuits;

one or more contact pads within said integrated circuit on said first
surface;

one or more electrically conductive materials placed in communication
with said bonding pad; and

5 said electrically conductive materials being in a channel in the direction of said
second surface or said region.

[0028] 5. The integrated circuit of claim 4 wherein a barrier material is placed between
said conductive materials and said channel surfaces.

[0029] 6. The integrated circuit of claim 5 wherein said conductive material surrounded
10 by said barrier material is contained in a channel in said semiconductor
wafer and said channel connects said front surface bonding pad to
said second surface or said separation region after a portion of said
known thickness has been removed.

[0030] 7. A method for producing integrated circuit devices including the steps of:

15 producing a plurality of integrated circuits on a wafer having first and
second planar surfaces, each of the integrated circuits including
regions for a multiplicity of bonding pads;

forming channels connecting said bonding pad regions on said first
surface to said second surface;

20 forming a barrier on surface of said channels;

depositing an electrically conductive material on said barriers in said
channels;

forming bonding pads in said bonding pad regions; and

forming electrical connections between said electrically conductive material and said bonding pads.

[0031] 8. A method for producing integrated circuit devices including the steps of:

5 producing a plurality of integrated circuits on a wafer having first and second planar surfaces, each of the integrated circuits including regions for a multiplicity of bonding pads;
forming channels in said bonding pad regions on said first surface extending a partial distance toward said second surface;
10 forming a barrier on surface of said channels;
depositing an electrically conductive material on said barriers in said channels;
forming bonding pads in said bonding pad regions;
forming electrical connections between said electrically conductive material and said bonding pads; and
15 thinning said wafer from said second surface until said conductive material in said channels is exposed on the thinned wafer's newly formed second surface.

20 [0032] 9. A method for producing integrated circuit devices including the steps of:

producing a plurality of integrated circuits on a wafer having first and second planar surfaces, each of the integrated circuits including regions for a multiplicity of active circuit elements;

forming channels from said second surface extending a partial distance
toward said first surface in thermal communication with said active
device regions;
forming a barrier on surface of said channels; and
5 depositing a thermally conductive material on said barriers in said
channels.

[0033] 10. The method of claim 9 wherein said thermally conductive material has a
thermal conductivity higher than the wafer material.

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[0034] 11. A mask set for producing integrated circuit devices comprising regions for:
producing a plurality of integrated circuits on a wafer having first and
second planar surfaces, each of the integrated circuits including
regions for a multiplicity of bonding pads;
15 forming channels in said bonding pad regions on said first
surface extending toward said second surface; and
forming electrical connections between said channel regions and said
bonding pad regions.

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20 [0035] 12. A design file on computer readable medium containing design rules for
producing integrated circuit devices on a wafer having first and second
planar surfaces, each of the integrated circuits including regions for
a multiplicity of bonding pads and said rules comprising:

guide lines for placing channels in said bonding pad regions on
said first surface extending toward said second surface; and
guide lines for interconnecting said channels to said bonding pad regions.